(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
105013

U.S. APPLICATION NO.
(if known, sec 37 C.F.R.1.5)
09/674924

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NOV 0 8 2000
PATENT & TRADEMARK OFFICE

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/01388	March 8, 2000	March 11, 1999

TITLE OF INVENTION
FLEXIBLE INTERCONNECT SUBSTRATE, FILM CARRIER, TAPE-SHAPED SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

APPLICANT(S) FOR DO/EO/US
Masahiko YANAGISAWA

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☒ Other items or information: Request for Approval of Drawing Corrections

529 Rec'd PCT/PTC 08 NOV 2000

U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/674924	INTERNATIONAL APPLICATION NO. PCT/JP00/01388	ATTORNEY'S DOCKET NUMBER 105013

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO $1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) .....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	24 - 20 =	4	X $ 18.00	$72	
Independent Claims	1 - 3 =	0	X $ 80.00	$	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$932	
Reduction by 1/2 for filing by small entity, if applicable.			-	$	
SUBTOTAL =				$932	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)).			+	$	
TOTAL NATIONAL FEE =				$932	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 113506 in the amount of $932 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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NAME: Joel S. Armstrong
REGISTRATION NUMBER: 36,430

(1390 Rev.10-00)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masahiko YANAGISAWA

Application No.: U.S. National Stage of PCT/JP00/01388

Filed: November 8, 2000 Docket No.: 105013

For: FLEXIBLE INTERCONNECT SUBSTRATE, FILM CARRIER, TAPE-SHAPED SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

Page 18, lines 5 and 6, change "reference numerals 46" to --reference numerals 48--.

Page 21, line 27, change "Fig. 5" to --Fig. 4--.

Page 22, line 27, change "A portable telephone 80" to --A portable telephone 180--.

Page 23, line 2, change "This portable telephone 80" to --This portable telephone 180--.

line 4, change "A notebook-sized personal computer 90" to --A notebook-sized personal computer 190--.

Page 24, line 15, change "the basic substrate 10" to --the base substrate 80--.

line 20, change "the basic substrate 90" to --the base substrate 80--.

line 2, change "the basic substrate 90" to --the base substrate 80--.

IN THE CLAIMS:

Please amend claim 22 and 23 as follows:

Claim 22, line 4, change "any one of claims 1 to 9" to --claim 1--.

Claim 23, lines 4 and 5, change "any one of claims 1 to 9" to --claim 1--.

REMARKS

Claims 1-24 are pending. By this Preliminary Amendment, the specification is amended, and claims 22 and 23 are amended to eliminate multiple dependencies. Prompt and favorable examination on the merits is respectfully solicited.

Respectfully submitted,

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Date: November 8, 2000
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Masahiko YANAGISAWA

Application No.: U.S. National Stage of PCT/JP00/01388

Filed: November 8, 2000 Docket No.: 105013

For: FLEXIBLE INTERCONNECT SUBSTRATE, FILM CARRIER, TAPE-SHAPED SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

REQUEST FOR APPROVAL OF DRAWING CORRECTION(S)

Director of the U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

The Examiner is requested to review and approve the proposed corrections to Figures 1, 7, and 8, marked in red on the attached copy of such drawing figures.

Upon approval by the Examiner, and upon allowance of this application, the formal drawings will be corrected.

Respectfully submitted,

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Registration No. 27,075

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Date: November 8, 2000

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sed Amended Drawings Epus-2192 1/2

FIG. 1

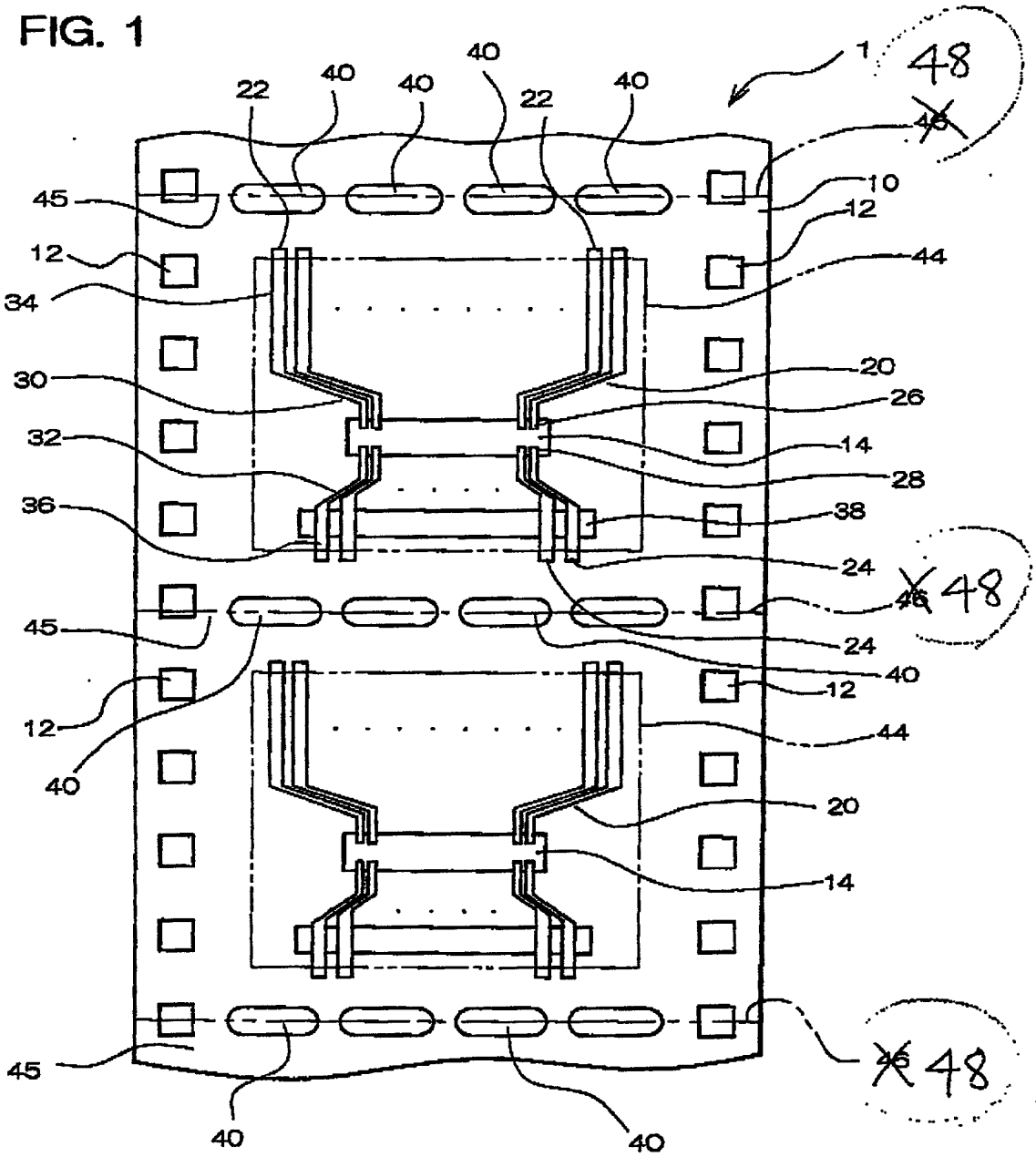


FIG. 7

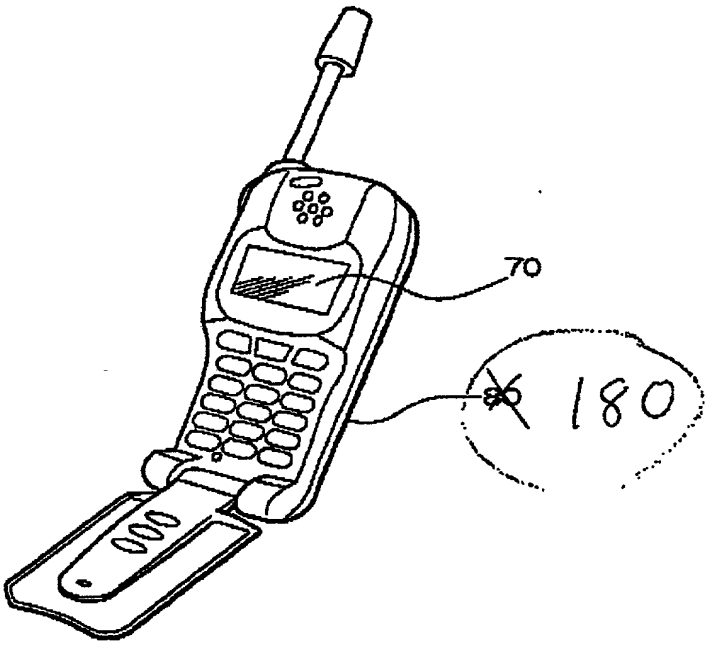
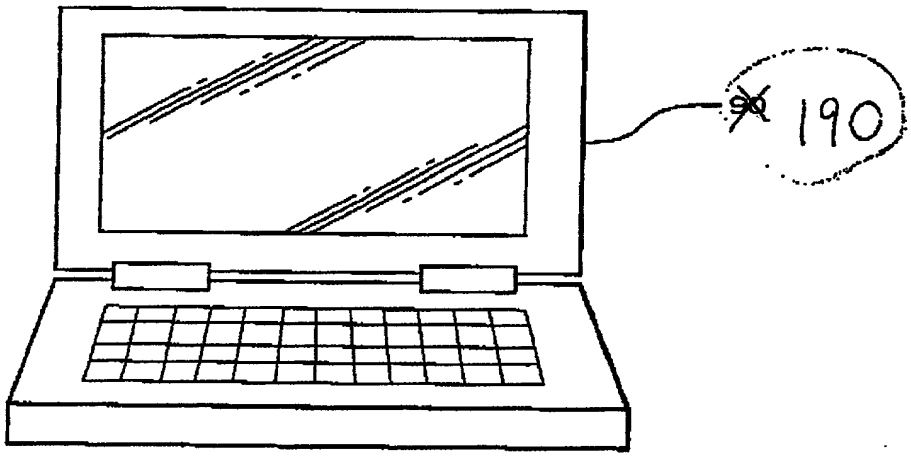


FIG. 8



FLEXIBLE INTERCONNECT SUBSTRATE, FILM CARRIER, TAPE-SHAPED SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

TECHNICAL FIELD

The present invention relates to a flexible interconnect substrate, a film carrier, a tape-shaped semiconductor device, a semiconductor device and a method of fabrication thereof, and a circuit board, together with electronic equipment.

BACKGROUND ART

The tape automated bonding (TAB) method is known in the art for mounting semiconductor chips onto a flexible interconnect substrate. Leads are formed on the flexible interconnect substrate and these leads are connected to pads of the semiconductor chips.

With this TAB method, the flexible interconnect substrate is curved and reel-to-reel processing is performed thereon, but when such a flexible interconnect substrate is wound onto a reel, the leads thereof may become bent.

DISCLOSURE OF THE INVENTION

The present invention was devised to solve this problem and has as an objective thereof the provision of a flexible interconnect substrate, a film carrier, a tape-shaped semiconductor device, a semiconductor device and a method of

manufacturing the same, a circuit board, and electronic equipment that make it possible to prevent bending of the leads.

(1) A flexible interconnect substrate in accordance with the present invention comprises: a tape-shaped base substrate; and an interconnect pattern formed on the base substrate,

wherein the base substrate includes: a first region in which a predetermined interconnect pattern has been formed and which will form a unit when separated from the base substrate; and a second region positioned next to the first region in the longitudinal direction of the base substrate; and

wherein the second region has a low-bending-resistance portion which is formed in a region that excludes a central portion of the second region in the widthwise direction of the base substrate, for ensuing that the second region bends more readily in the direction in which the longitudinal axis of the base substrate bends, in comparison with the first region.

This aspect of the present invention ensures that a region (a second region) that is designed to bend more readily is provided adjacent to a region (a first region) that is to be punched out. When the flexible interconnect substrate is bent, stresses therefore concentrate in this second region, and thus the stress concentrations avoid the first region. This suppresses any bending of the interconnect pattern within the first region.

In addition, the low-bending-resistance portion is formed in a region that excludes the central portion in the widthwise direction of the base substrate within the second

region, making it possible to suppress excessive deformation of the second regions, even when the base substrate is pulled in the longitudinal direction.

(2) In this flexible interconnect substrate,

the low-bending-resistance portion may be one of through-holes, cuts, and a thinner portion.

A thinner portion makes the bending resistance lower, and through-holes or cuts reduce the bending resistance to zero. Thus the term "low-bending-resistance portion" includes any portion where the bending resistance is zero.

(3) In this flexible interconnect substrate, the configuration may be such that:

a high-bending-resistance portion is formed in each of the first region and the central portion of the second region in the widthwise direction of the base substrate;

the high-bending-resistance portion is formed to avoid a region that excludes the central portion of the second region in the widthwise direction of the base substrate; and

the region avoided by the high-bending-resistance portion forms a relatively low-bending-resistance portion.

This configuration is not limited to a case in which the low-bending-resistance portion is formed deliberately; it could also apply to cases in which the bending resistance is reduced by an increase in the bending resistance in all other portions.

(4) In this flexible interconnect substrate, the configuration may be such that:

a hole is formed in the first region of the base substrate; and

a portion of the interconnect pattern is positioned within that hole.

With this configuration, the portion of the interconnect pattern that is positioned within the hole is not supported by the base substrate, but since the stresses concentrate in the second region, as described above, the bending of a lead that is positioned within the first region is suppressed.

(5) In this flexible interconnect substrate,

the second region may be formed to bend more readily than the first region that bends readily due to the formation of the hole.

The formation of the hole makes it possible for the first region to bend more readily, but the second region bends even more readily than that first region, making it possible to avoid stress concentrations in the first region.

(6) In this flexible interconnect substrate,

a plurality of the low-bending-resistance portions may be formed in a straight line within the second region, across the width of the base substrate.

This makes it easier for the second regions to bend.

(7) In this flexible interconnect substrate,

the plurality of low-bending-resistance portions may be disposed on two edge portion sides of the base substrate, symmetrically with respect to the center in the widthwise direction of the base substrate.

This ensures that the substrate bends readily in a manner that is symmetrical across the width thereof.

(8) In this flexible interconnect substrate,

the plurality of low-bending-resistance portions may be disposed on two edge portion sides of the base substrate, asymmetrically with respect to the center in the widthwise direction of the base substrate.

This makes it possible to ensure that the substrate bends readily in a manner that is asymmetrical across the width thereof.

(9) In this flexible interconnect substrate,

the interconnect pattern may be formed to be offset towards either of two edge portions of the base substrate, with respect to the center in the widthwise direction of the base substrate.

This makes it possible to dispose the interconnect pattern in correspondence with a asymmetrical mode of bending.

(10) A tape-shaped semiconductor device in accordance with the present invention comprises: the previously described flexible interconnect substrate; and a semiconductor chip connected electrically to the interconnect pattern of the base substrate.

With this aspect of the present invention, all the above described details of the flexible interconnect substrate apply.

(11) Another tape-shaped semiconductor device in accordance with the present invention comprises:

the previously described flexible interconnect

substrate; and

a semiconductor chip which is disposed offset towards either of two edge portions of the base substrate, with respect to the center in the widthwise direction of the base substrate, and which is connected electrically to the interconnect pattern of the base substrate.

With this aspect of the present invention, all the above described details of the flexible interconnect substrate apply.

(12) A semiconductor device in accordance with the present invention has a shape obtained by punching out the base substrate of the previously described tape-shaped semiconductor device along an outline that surrounds the semiconductor chip.

This semiconductor device is not limited to one obtained by punching out the tape-shaped semiconductor device as described above, but it can also apply to semiconductor devices that have the same configuration and shape as punched-out devices. Details of the flexible interconnect substrate are as described previously.

(13) A circuit board in accordance with the present invention is connected electrically to the previously described semiconductor device.

(14) Electronic equipment in accordance with the present invention comprises the previously described semiconductor device.

(15) A method of manufacturing a semiconductor device in accordance with the present invention comprises the steps of:

winding the previously described flexible interconnect substrate onto a reel in preparation; and then pulling the flexible interconnect substrate out from the reel.

In this aspect of the present invention, the base substrate bends as the flexible interconnect substrate is wound up, but it is possible to suppress bending of the interconnect pattern because the previously described flexible interconnect substrate is used therefore.

(16) Another method of manufacturing a semiconductor device in accordance with the present invention comprises the steps of: winding a tape-shaped semiconductor device which comprises the previously described flexible interconnect substrate and a semiconductor chip connected electrically to the interconnect pattern of the flexible interconnect substrate, onto a reel in preparation; and then pulling the tape-shaped semiconductor device out from the reel.

In this aspect of the present invention, the base substrate bends as the flexible interconnect substrate is wound up, but it is possible to suppress bending of the interconnect pattern because the previously described flexible interconnect substrate is used therefore.

(17) In this method of manufacturing a semiconductor device, the flexible interconnect substrate may be punched out at the first region, during the step of pulling the tape-shaped semiconductor device out from the reel.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 shows a flexible interconnect substrate in accordance with an embodiment of the present invention.

Figs. 2A and 2B show a usage state of the flexible interconnect substrate in accordance with this embodiment of the present invention.

Fig. 3 shows a method of manufacturing a tape-shaped semiconductor device in accordance with an embodiment of the present invention.

Fig. 4 shows a tape-shaped semiconductor device in accordance with an embodiment of the present invention.

Fig. 5 shows a method of manufacturing a semiconductor device in accordance with an embodiment of the present invention.

Fig. 6 shows a circuit board in accordance with an embodiment of the present invention.

Fig. 7 shows an item of electronic equipment having a semiconductor device in accordance with this embodiment.

Fig. 8 shows another item of electronic equipment having a semiconductor device in accordance with this embodiment.

Fig. 9 shows a modification of a flexible interconnect substrate in accordance with an embodiment of the present invention.

Figs. 10A and 10B show another modification of the flexible interconnect substrate in accordance with an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

Preferred embodiments to which this invention are applied will be described below with reference to the accompanying figures, but it should be noted that the present invention is not limited to the embodiments described herein.

Flexible Interconnect substrate

A flexible interconnect substrate in accordance with an embodiment of this invention is shown in Fig. 1. This flexible interconnecting substrate 1 comprises a base substrate 10 and a plurality of interconnect patterns 20. The flexible interconnecting substrate 1 could be handled by being wound onto a reel 46, as shown in Fig. 2A. If the TAB technique is to be applied, the flexible interconnect substrate is a substrate for TAB (a film carrier tape), but it is not limited thereto and thus could equally well be a substrate for chip-on-film (COF) packaging or a substrate for chip-on-board (COB) packaging.

The base substrate 10 is a base material of a tape-shaped form that acts as a support member for the interconnect patterns 20. The base substrate 10 has flexibility. The base substrate 10 is frequently formed of a polyimide resin, but other known materials can be used therefor. If a plurality of sprocket holes 12 are formed in the lengthwise direction along both sides of the base substrate 10, with respect to the widthwise direction, the flexible interconnect substrate can be moved out by an engagement with sprockets (not shown in the figure).

If the TAB technique is to be used, one device hole 14 (or a plurality thereof overall) is formed in the interconnect

patterns 20 on the base substrate 10. Bonding between a semiconductor chip 60 (see Fig. 4) and electrical connection portions therefor (such as inner leads 26 and 28) can be done through this device hole 14. The shape of the device hole 14 is not particularly limited, so it could be of a size sufficient to completely accommodate the semiconductor chip 60, or of a size that accommodates only part thereof.

A plurality of the interconnect patterns 20 are formed on the base substrate 10. The base substrate 10 supports the interconnect patterns 20. With a flexible interconnect substrate 1 that has a three-layer substrate, the interconnect patterns 20 are attached to the base substrate 10 by an adhesive (not shown in the figure). With a flexible interconnect substrate that has a two-layer substrate, the interconnect patterns 20 are formed on the base substrate 10 with no adhesive therebetween.

The interconnect patterns 20 could be formed aligned in the longitudinal direction of the tape-shaped base substrate 10, or they could be formed across the width thereof, or they could be formed in a matrix form (aligned in both the longitudinal direction and the widthwise direction). The interconnect patterns 20 often have the same shape, but they can also be of different shapes. For example, a interconnect pattern group that is configured of an array of n interconnect patterns 20 of n different shapes could be formed repeatedly.

The interconnect patterns 20 can be formed of multiple layers of any of copper (Cu), chrome (Cr), titanium (Ti), nickel

(Ni), or titanium-tungsten (Ti-W); or of an single layer of any of those metals. The interconnect patterns 20 are preferably plated with a material such as solder, tin, gold, or nickel. If metal plating is performed in such a manner that a eutectic is created, it is preferable that metal bonding is easy to achieve. To facilitate the electrical plating of a plurality of the interconnect patterns 20, they could be connected electrically by plating leads (not shown in the figure).

Each of the interconnect patterns 20 has a plurality of interconnects 22 and 24. More specifically, a plurality of interconnects 22 is formed in the longitudinal direction of the base substrate 10 on a first side of the device hole 14 (the upper side in Fig. 1) and a plurality of interconnects 24 is formed on a second side thereof (the lower side in Fig. 1).

Each of the interconnects 22 and 24 comprises an inner lead 26 or 28 at one end thereof, an oblique portion 30 or 32 that extends in a direction of an increasing spacing, and an end portion 34 or 36 at the other end thereof.

The inner leads 26 and 28 protrude into the device hole 14. The inner leads 26 and the inner leads 28 are each formed to be mutually parallel, and could be formed to extend in the longitudinal direction of the base substrate 10. The inner leads 26 and 28 act as electrical connection portions with the semiconductor chip 60.

The oblique portions 30 and 32 are formed to be inclined with respect to the direction in which the spacing of the inner leads 26 and 28 increases. The oblique portions 30 and 32 could

be formed to have either a linear shape or a curved shape.

The end portions 34 and 36 are set to extend from the oblique portions 30 and 32, on the opposite side from the inner leads 26 and 28. Each group of end portions 34 and end portions 36 is formed to be mutually parallel and could be formed to extend in the longitudinal direction of the base substrate 10. At least one of the width and pitch of the end portions 34 and 36 can be formed to be larger than that of the inner leads 26 and 28. The end portions 34 and 36 are connected electrically to other electrical components. In the example shown in Fig. 1, the end portions 36 of the interconnects 24 are formed to straddle an outer lead hole 38, and the portions of the end portions 36 that are within the outer lead hole 38 act as outer leads.

The base substrate 10 comprises a plurality of first regions 44 and a plurality of second regions 45. Each first region 44 is a region that is to be punched out. In the example shown in Fig. 1, each first region 44 is positioned in a central portion across the width of the base substrate 10. In other words, each first region 44 is positioned inward of edge portions of the base substrate 10 so that, when the base substrate 10 is punched out at the first region 44, both edge portions of the base substrate 10 are left, with respect to the width thereof. Alternatively, each first region 44 could comprise one side edge of the base substrate 10, or it could comprise the entire portion across the width of the base substrate 10 (from one side edge to the other side edge). At least part of each interconnecting pattern 20 is formed within one of the first regions 44. A

plurality of the first regions 44 (not necessarily all of them) are positioned in a line along the longitudinal direction of the tape-shaped base substrate 10. Note that the semiconductor chip 60 (see Fig. 4) is mounted on one of the first regions 44 and the device hole 14 is formed within this first region 44.

The second regions 45 are positioned between the first regions 44. More specifically, each second region 45 is positioned between two of the first regions 44 that are adjacent in the longitudinal direction of the base substrate 10. Each second region 45 is a part of the base substrate 10 and comprises the entire portion thereof across the width thereof (from one side edge to the other side edge).

Apertures such as through-holes, slits, or cuts are not formed in a central portion of each second region 45 in the widthwise direction of the base substrate 10. In other words, there is some of the material at the central portion of the second region 45 in the widthwise direction of the base substrate 10. This makes it possible to ensure that deformation is not too great, even when the base substrate is pulled. Note that the material that does exist in the central portion of the second region 45 in the widthwise direction of the base substrate 10, could be a material that supports the interconnecting patterns 20 (such as a polyimide resin) or it could be a different material (such as a single layer of a weak material or a hard material). Regardless of what type of material is used, this material forms part of the base substrate 10. Alternatively, the portion within the central portion of the second region 45 in the widthwise

direction of the base substrate 10 could have a different thickness from the portion that supports the interconnect pattern 20. That is to say, the central portion of the second region 45 in the widthwise direction of the base substrate 10 could be formed to be either thinner or thicker.

At least one low-bending-resistance portion 40 is formed within each second region 45 (in Fig. 1, there are a plurality of low-bending-resistance portions 40). This low-bending-resistance portion 40 is designed to ensure that the second region 45 bends more readily than the first region 44. More specifically, each low-bending-resistance portion 40 bends easily in a direction such that the second region 45 bends along the longitudinal axis of the base substrate 10 (such as when the assembly is being wound on a reel). This ensures that when the base substrate 10 is being bent, such as when it is being wound, bending stresses concentrate in the second regions 45, avoiding bending stress concentrations at the first regions 44. As a result, there is little bending of the interconnecting patterns 20 within the first regions 44.

The low-bending-resistance portions 40 shown in Fig. 1 are slits, where these slits are formed to extend across the width of the base substrate 10. These low-bending-resistance portions 40 could also be through-holes, cuts, or thinner portions. Alternatively, the low-bending-resistance portions 40 could be formed of a material that is weaker (and thus more bendable) than the material of the first regions 44. If the low-bending-resistance portions 40 are apertures such as slits,

the bending resistance of the low-bending-resistance portions 40 is zero. If there is some material in the low-bending-resistance portions 40, such as in thinner portions, the low-bending-resistance portions 40 will have some bending resistance.

A plurality of the low-bending-resistance portions 40 could be formed at intervals across the width of the base substrate 10. In such a case, the low-bending-resistance portions 40 could be formed in a straight line across the width of the base substrate 10. In the example shown in Fig. 1, a plurality of the low-bending-resistance portions 40 are disposed symmetrically on either side with respect to the center of the width of the base substrate 10. In this case, "symmetrical" means that they are symmetrical in both shape and position, and the bending resistances thereof are also symmetrical.

Alternatively, one low-bending-resistance portion 40 could be formed across the width of the base substrate 10, straddling the center thereof, provided that the low-bending-resistance portion 40 is not apertures alone. The entire second region 45 could also be formed as the low-bending-resistance portion 40.

The second region 45 in which the low-bending-resistance portion 40 is formed preferably bends more readily than regions of the adjacent first regions 44 that comprise portions of the interconnecting patterns 20 that are more likely to deform. Portions of the interconnecting patterns 20 that are not

supported directly by the base substrate 10 are more likely to deform. Examples include portions of the interconnecting patterns 20 which are positioned within holes (such as the inner leads 26 and 28 and the end portions 36 that form outer leads, which are positioned within the device hole 14 and the outer lead hole 38). It is therefore preferable to ensure that the second region 45 bends more readily than the edge portions of the holes.

A protective film 42 (see Fig. 5) could be provided on top of the interconnecting patterns 20. The protective film 42 protects the interconnect patterns 20 from oxidation or the like. The protective film 42 could be formed of a resin such as solder resist. The protective film 42 is provided to cover is provided to cover the interconnect pattern 20 except for those portions in electrical contact with other components such as a semiconductor chip (such as the inner leads, external pins, and outer leads). The protective film 42 is provided to cover the interconnect patterns 20 except for those portions in electrical contact with other components such as a semiconductor chip (such as the inner leads 26 and 28, external pins, and outer leads).

Each of the interconnecting patterns 20 is used to fabricate one semiconductor device, and the flexible interconnecting substrate 1 is used to fabricate a plurality of semiconductor devices. The base substrate 10 is provided with a plurality of the first regions 44. Each first region 44 is punched out of the base substrate 10 to form a semiconductor

device. One interconnecting pattern 20 is formed in each first region 44. The interconnecting pattern 20 could be formed to protrude from the first region 44. In other words, part of each interconnecting pattern 20 could be positioned outside the corresponding first region 44.

A usage state of the flexible interconnect substrate in accordance with this embodiment of the invention is shown in Fig. 2A, with a side view of part of the flexible interconnect substrate being shown in Fig. 2B. As shown in Fig. 2A, the flexible interconnecting substrate 1 is wound onto the reel 46. In this case, the axial line of the base substrate 10 in the longitudinal direction bends but the low-bending-resistance portions 40 are formed in the second regions 45 of the base substrate 10. Thus the second regions 45 formed in the low-bending-resistance portions 40 bend greatly because the bending stresses concentrate in those positions, so that there is little bending of the first regions 44 in which the low-bending-resistance portions 40 are not formed, as shown in Fig. 2B. The interconnecting patterns 20 are formed in the first regions 44 where there is little bending, as shown in Fig. 1, which makes it possible to suppress bending of the interconnecting patterns 20.

It is therefore possible to pull the flexible interconnecting substrate 1 off from the reel 46 and perform processing thereon, or perform reel-to-reel processing thereon.

Film Carrier

In a film carrier in accordance with another embodiment to which the present invention is applied, the flexible interconnect substrate of Fig. 1 is cut along lines in the widthwise direction (the broken lines indicated by reference numerals 46 in Fig. 1). For example, the film carrier is a piece of film cut from the above described flexible interconnect substrate. Note that the positions at which the flexible interconnect substrate is cut are not particularly limited. In the example shown in Fig. 1, both sides of one interconnect patterns 20 act as cutting positions, but both sides of a plurality of interconnect patterns 20 could equally well be used as cutting positions.

Method of Manufacturing a Tape-Shaped Semiconductor Device

The description now turns to a method of manufacturing a tape-shaped semiconductor device in accordance with an embodiment to which the present invention is applied, with reference to Fig. 3.

As shown in Fig. 3, the flexible interconnecting substrate 1 has been previously wound onto the reel 46 and is conveyed therefrom to a bonding unit 50 for mounting semiconductor chips. A buffer region (slack portion) 52 is provided between the reel 46 and the bonding unit 50, so that the amount by which the reel 46 is drawn out ensures that semiconductor chips can be mounted on the flexible interconnecting substrate 1, not necessarily in

synchronization with the tact time of the bonding unit 50.

Since the flexible interconnecting substrate 1 is in a state such that it dangles under its own weight within the buffer region 52, it bends due to its own weight at the lowermost position thereof and thus bending stresses are applied to the flexible interconnecting substrate 1. However, the flexible interconnecting substrate 1 in accordance with this embodiment of the invention is provided with the low-bending-resistance portions 40, so these bending stresses concentrate at the low-bending-resistance portions 40. It is therefore possible to prevent the bending stresses from concentrating at the electrical connection portion (such as the inner leads 26 and 28), preventing the occurrence of cracks and broken wires.

Tape-Shaped Semiconductor Device

A tape-shaped semiconductor device in accordance with a further embodiment to which this invention is applied is shown in Fig. 4, which is a cross-sectional view taken along a line across the width of the 10.

This tape-shaped semiconductor device has the above described flexible interconnecting substrate 1 and a plurality of semiconductor chips 60 that are connected electrically to the interconnect patterns 20 thereof.

The planar shape of each semiconductor chip 60 is generally quadrangular, but it could be either rectangular or square. A plurality of electrodes is formed on one surface of each semiconductor chip 60. The electrodes are aligned along

at least one edge (or two or four edges, if more than one) of the surface of the semiconductor chip. If the outer shape of each semiconductor chip 60 is rectangular, electrodes could be arrayed in the longer direction thereof, as in an IC for a liquid crystal drive by way of example, or they could be arrayed in the shorter direction thereof. In some cases, the electrodes may be arrayed at an end portion of the surface of each semiconductor chip 60, or they may be arrayed at a central portion thereof. The electrodes are often configured of pads that are formed thinly and flat of a material such as aluminum, with bumps formed on top thereof. If bumps are not formed, the pads alone become electrodes. A passivation film (not shown in the figure) is formed over the semiconductor chips, except for at least part of the electrodes. The passivation film can be formed of a material such as SiO_2, SiN, or polyimide resin, by way of example.

The electrodes of the semiconductor chips 60 could be bonded to the inner leads 26 and 28 of the interconnect patterns 20 through the device hole 14, by applying the TAB technique.

Alternatively, face-down bonding of the semiconductor chips 60 could be employed, if a flexible interconnect substrate with no device hole 14 is used. In such a case, the flexible interconnect substrate could be a substrate wherein the active surface of each semiconductor chip 60 (the surface on which electrodes are formed) and the base substrate are on opposite sides, in other words, chip-on-film (COF) mounting.

Alternatively, if wire bonding or the like is to be

employed, each semiconductor chip 60 could be bonded face-up. In such a case, the active surface of the semiconductor chip 60 (the surface on which electrodes are formed) is orientated in the same direction as the mounting surface of the base substrate of the flexible interconnect substrate. For example, the electrodes of the semiconductor chip 60 could be connected to the interconnect pattern 20 by wires (fine wires) of metal to give a face-up-mounted substrate.

The tape-shaped semiconductor device could have a seal portion 62. The seal portion 62 seals in at least the electrical connection portions between the electrodes of the semiconductor chip 60 and the interconnect pattern 20 (such as the inner leads 26 and 28). This seal portion 62 is often formed of resin.

In addition, the end portions of the protective film 42 preferably overlap the seal portion 62 at each boundary between portions of the interconnecting pattern 20 that are not covered by the protective film 42 and portions that are covered thereby (see Fig. 5). This makes it possible to prevent exposure of the interconnect pattern 20. The seal portion 62 could be provided by potting or it could be provided by a transfer mold.

Semiconductor Device and Method of Manufacturing the Same

A semiconductor device and method of manufacturing the same in accordance with a still further embodiment to which this invention is applied is shown in Fig. 5. This semiconductor device is formed by cutting the tape-shaped semiconductor device of Fig. 5 along lines that extend in the widthwise

direction. The tape-shaped semiconductor device could be cut on both sides of one interconnect pattern 20, using cutting tools 64 (such as cutters or a punch), as shown in Fig. 5 by way of example. These cutting positions could be those indicated by the broken line 48 in Fig. 1.

The semiconductor device in accordance with this embodiment of the invention could be formed by punching out the base substrate 10 of the above described tape-shaped semiconductor device. The position of the punching could be along the outline of one interconnect pattern 20.

Semiconductor Device and Circuit Board

A circuit board in accordance with yet another embodiment to which this invention is applied is shown in Fig. 6. As shown in Fig. 6, a semiconductor device 72 as described above is connected electrically to a circuit board 70. The circuit board 70 could be a liquid crystal panel, by way of example. The semiconductor device 72 is formed by punching out the base substrate 10 of the tape-shaped semiconductor device around the outline that encompasses the semiconductor chip 60.

The base substrate 10 of the semiconductor device 72 could also be provided with bends, as shown in Fig. 6. For example, the base substrate 10 could be made to bend around an end portion of the circuit board 70.

Electronic Equipment

A portable telephone 80 is shown in Fig. 7 as an example

of electronic equipment having a semiconductor device to which this invention is applied. This portable telephone 80 has the circuit board 70 (liquid crystal panel) to which this invention is applied. A notebook-sized personal computer 90 having a semiconductor device (not shown in the figure) to which this invention is applied is shown in Fig. 8.

Note that the "semiconductor chip" that is a structural component of the present invention could be replaced by an "electronic element," and electronic elements (either active elements or passive elements) can be mounted on a flexible interconnect substrate or film carrier to fabricate an electronic component, in a manner similar to that of a semiconductor element. Examples of electronic components fabricated by using such electronic elements include optical elements, resistors, capacitors, coils, oscillators, filters, temperature sensors, thermistors, varistors, variable resistors, or fuses, by way of example.

Modifications

A flexible interconnect substrate in accordance with a modification of an embodiment to which the present invention is applied is shown in Fig. 9. This flexible interconnect substrate comprises a base substrate 80 and interconnect patterns 90. The base substrate 80 comprises a first region 82 and a second region 84, and low-bending-resistance portions 86 and 88 are formed in the second region 84.

The low-bending-resistance portions 86 and 88 are

disposed asymmetrically on either side with respect to the central portion in the widthwise direction of the base substrate 80. In this case, "asymmetrically" means either that the shapes, numbers, or positions thereof are asymmetrical or that the bending resistances thereof are asymmetrical. In the example shown in Fig. 9, a plurality of low-bending-resistance portions 86 are formed on the side of one edge portion and a small number (such as one) of low-bending-resistance portions 88 is formed on the side of another edge portion thereof. The low-bending-resistance portions 86 on one side are circular, by way of example. The other low-bending-resistance portions 88 are elongated holes, by way of example, that are formed to extend across the width of the base substrate 80. Since the asymmetrical low-bending-resistance portions 86 and 88 are formed in the base substrate 10 in this manner, the base substrate 80 can be made to bend readily in a asymmetrical manner.

The interconnect patterns 90 are positioned offset towards one edge portion, with reference to the central portion in the widthwise direction of the base substrate 90. The interconnect patterns 90 could be formed offset towards the parts of the low-bending-resistance portions 86 and 88 that bend more readily, by way of example. This ensures that portions within each second region 84, where bending stresses readily concentrate, are close to the interconnect patterns 90, thus reducing the bending in the interconnect patterns 90. In this case, each first region 82 is positioned offset towards one edge

portion with respect to the central portion in the widthwise direction of the base substrate 90.

In all other respects, details given with reference to the previously described embodiments apply also to this modification.

A flexible interconnect substrate in accordance with another modification of an embodiment to which the present invention is applied is shown in Figs. 10A and 10B. This flexible interconnect substrate has the same configuration as the base substrate 10 that was described with reference to Fig. 1. Fig. 10A is a cross-sectional view of a first region 44 of the base substrate 10 and Fig. 10B is a cross-sectional view of a second region 45 of the base substrate 10. The device hole 14 and the sprocket holes 12 are formed in the base substrate 10.

High bending resistance portions 100 are formed on top of the base substrate 10. The high-bending-resistance portions 100 are designed to have a bending resistance that is higher than that of the region on which they are formed, and are preferably more rigid than the base substrate 10. The high-bending-resistance portions 100 could be formed of a substrate that is more rigid than the base substrate 10 or they could be formed of a resist (solder resist), by way of example. Alternatively, the formation of the high-bending-resistance portions 100 ensures that, if the bending resistance of the thus formed region is increased, the rigidity thereof could make use of the high-bending-resistance portions 100 of a rigidity that is the same as or less than that of the base substrate 10.

As shown in Fig. 10A, the high-bending-resistance portions 100 are formed in the first region 44, but they are also formed to exclude portions of the second region 45. The high-bending-resistance portions 100 are formed within a central portion in the widthwise direction of the base substrate 10, even in the second region 45. The parts of the second region 45 in which the high-bending-resistance portions 100 are not formed act as relatively low-bending-resistance portions 140. In other words, the low-bending-resistance portions 140 are formed in parts of the second region that avoid the central portion in the widthwise direction of the base substrate 10.

The low-bending-resistance portions 140 are formed in regions of the second region 45 that avoid the central portion in the widthwise direction of the base substrate 10. The formation of the low-bending-resistance portions 140 makes the second region 45 more likely to bend than the first region 44 in the direction in which the longitudinal axis curves.

Details that have been described with reference to Fig. 10 can also be applied to the previously described embodiment and modification of the present invention.

The description now turns to an example in which the present invention is applied to film carrier tape. The form of the film carrier tape in accordance with this embodiment has already been described with reference to Fig. 1. The film carrier tape in accordance with this embodiment shown in Fig. 1 is fabricated by first forming the device hole 14 and the outer lead hole 38 in a tape-shaped substrate (the base substrate 10)

that has flexibility, then providing the interconnect patterns 20 around these holes.

The tape-shaped substrate is a film made of a polyimide, a plurality of sprocket holes 12 is provided at uniform spacing in the longitudinal direction along both edges across the width of the tape-shaped substrate, so that the tape-shaped substrate can be moved in the direction of transfer by the engagement of sprockets (not shown in the figure) provided in the transfer path.

A plurality of punch-out regions (the first regions 44) are provided in this tape-shaped substrate along the longitudinal direction thereof, to correspond to the outer shapes of punch-out regions for the film carrier.

The device hole 14, which is of a size just sufficient to accommodate the semiconductor chip 60 (see Fig. 4), and the outer lead hole 38, which is adjacent to this device hole 14, are provided within each of these punch-out regions, and slits (as an example of the low-bending-resistance portions 40) that form bendable portions are provided on the outer sides of the punch-out regions, in other words, between adjacent punch-out regions. The interconnect pattern 20 is formed between the device hole 14 and the outer lead hole 38. One end of the interconnect pattern 20 is made to protrude from the edge of the device hole 14, to act as the inner leads 28 for the input side which are intended to connection pins that are formed in the surface of the semiconductor chip 60. The interconnect pattern 20 is drawn out to extend over the outer lead hole 38,

on the opposite side of the interconnect pattern 20 from that of the inner leads 28 for the input side. The parts of the interconnect pattern 20 that straddle the outer lead hole 38 act as outer leads which are intended to connection pins that are formed in an external substrate (not shown in the figures).

The inner leads 26 for the output side are formed on the opposite side of the device hole 14 from the inner leads 28 for the input side. The inner leads 26 for the output side are also formed to protrude in such a manner that there is a number thereof equivalent to the number of connection pins of the semiconductor chip 60. The interconnect pattern 20 that acts as one side-edge portion of the inner leads 26 for the output side are drawn out to extend to the opposite side on which the outer lead hole 38 is formed, the thus extended portion is subjected to solder plating to provide connections with another external substrate, so that solder lands are formed thereby.

The slits (as one example of the low-bending-resistance portions 40) that are formed between the punch-out regions (the first regions 44) are formed in a plurality of lateral rows in such a manner that the longitudinal direction thereof matches the widthwise direction of the tape-shaped substrate. The configuration is such that, when the tape-shaped substrate (the base substrate 10) is subjected to bending in the longitudinal direction thereof, the regions in which these slits are formed has the lowest bending resistance. In other words, if the shape of the slits when they are formed is set in such a manner that the proportion occupied by the slits across the width of the

tape-shaped substrate is greater than that of the holes in other regions, the dimensions of the substrate material is less than those in the other regions, making it possible to minimize bending resistance.

During the process of manufacturing the thus configured film carrier tape, the device hole 14, the outer lead hole 38, and the slits are punched out of the tape-shaped substrate simultaneously, then copper foil is laminated over the surface of the tape-shaped substrate, and the copper foil is exposed and etched to form the interconnect pattern 20. The film carrier tape that is fabricated by this sequence later accepts the semiconductor chip 60 in the device hole 14 and the inner leads 26 and 28 are connected electrically. The semiconductor chip 60 is then sealed into protective resin and the film carrier is punched out along the outer shape of the punch-out region. The semiconductor chip 60 thus forms a semiconductor device mounted on the film carrier.

The above described manufacturing process can have a number of fabrication lines within each step, instead of having the entire process running along the transfer direction of the tape-shaped substrate, as in a single fabrication line. The film carrier tape is wound onto the reel 46 in a roll at the far end of each predetermined fabrication line and also that reel 46 is placed at the start of the next-stage fabrication line, so that the film carrier tape can be sent out for the next-stage fabrication line.

Cross-sectional views of portions of the film carrier

tape when wound onto the reel 46 are shown in Figs. 2A and 2B. If the near end of the film carrier tape is attached to the core of the reel 46 and the film carrier tape is wound around that core, as shown in Fig. 2A, the film carrier tape forms a roll and the outer dimensions of that roll increases as the amount of tape wound thereon increases. In this case, the winding of the film carrier tape onto the reel 46 causes bending stresses to act thereon, but the provision of slits (the low-bending-resistance portions 40) in the film carrier tape ensures that the resistance to bending is low at the regions provided with those slits. This means that bending stresses concentrate at those portions and thus the film carrier tape is bent into a polygonal shape with the regions of the slits acting as vertices, as shown in Fig. 2B. For that reason, there is no concentration of stresses due to bending at the portions either side of the regions provided with slits, in other words, the regions in which the outer lead holes 38 are formed. It is therefore possible to prevent bending stress concentrations at the outer leads formed in each outer lead hole 38, thereby preventing the occurrence of cracking and breakage of the outer leads.

The form of the fabrication line in which the semiconductor chips 60 are mounted on the film carrier tape will now be described with reference to Fig. 3. The film carrier tape that is drawn out from the reel 46, as shown in Fig. 3, is inserted into the bonding unit 50 of this fabrication line, where the semiconductor chips 60 are mounted. The buffer region (slack

portion) 52 is provided between the reel 46 and the bonding unit 50, so that the amount by which the reel 46 is drawn out ensures that semiconductor chips 60 can be mounted on the flexible interconnecting substrate 1, not necessarily in synchronization with the tact time of the bonding unit 50.

Since the film carrier tape is in a state such that it dangles under its own weight within the buffer region 52, it bends due to its own weight at the lowermost position thereof and thus bending stresses are applied to the film carrier tape. However, the film carrier tape is provided with regions having slits and thus the bending resistance at those portions is small, so that bending stresses concentrate at those portions and thus the film carrier tape is bent into a polygonal shape with the regions of the slits acting as vertices. For that reason, there is no concentration of stresses due to bending at the portions either side of the regions provided with slits, in other words, the regions in which the outer lead holes 38 are formed. It is therefore possible to prevent bending stress concentrations at the outer leads formed in each outer lead hole 38, thereby preventing the occurrence of cracking and breakage of the outer leads.

In addition, the stresses are made to concentrate in the regions in which the slits (the low-bending-resistance portions 40) are formed, so that there are no bending stress concentrations on the punch-out regions (the first regions 44). There is therefor no deformation, not only of the outer leads but also of the inner leads 28 for the input side and the inner

leads 26 for the output side, making it possible to position the inner leads and the semiconductor chip accurately.

Note that this embodiment of the invention was described with reference to positions where semiconductor chips are mounted on a film carrier tape, but the present invention is not limited to such positions and similar effects can be obtained by the buffer region 52 for other locations at which bending stresses are applied to the film carrier tape.

In the method of manufacturing a film carrier tape in accordance with this embodiment of the invention, punch-out regions (the first regions 44) are set in sequence along the longitudinal direction of a tape-shaped substrate (the base substrate 10) that has flexibility, then bendable portions are provided between the punch-out regions in such a manner that the bending resistance thereof is less than that of the punch-out regions. Since the method of manufacturing film carrier tape in accordance with this embodiment of the invention ensures that the regions between the punch-out regions bend readily, any attempt to bend the film carrier tape causes the bending stresses concentrate at those bendable portions so that the film carrier tape bends at the bendable portions into a polygonal shape, thereby making it possible to prevent bending stress concentrations at the punch-out regions.

Note that it does not matter what is done at the bendable portions to reduce the bending resistance of the tape-shaped substrate, more specifically, there could equally well be slits formed in the lateral direction (the widthwise direction) of

the tape-shaped substrate, cuts introduced in the lateral direction of the tape-shaped substrate, or a lessening of the thickness of the tape-shaped substrate.

The method of manufacturing a film carrier tape in accordance with this embodiment of the invention also includes a process in which punch-out regions (the first regions 44) are set in sequence along the longitudinal direction of a tape-shaped substrate (the base substrate 10) that has flexibility, the device holes 14 and the neighboring outer lead holes 38 are formed within these punch-out regions, then the interconnect patterns 20 are formed, each with one end portion protruding from a device hole 14 and another end portion straddling an outer lead hole 38. Before the interconnect patterns 20 are formed, slits are formed between the punch-out regions. This ensures that the bending resistance of the tape-shaped substrate between the punch-out regions is less than the bending resistance of the regions in which are formed the outer lead holes 38 that are straddled by the interconnect patterns 20. When the film carrier tape itself bends, the resultant bending stresses concentrate between the punch-out regions, that is, at the regions in which the slits are formed, so that there are no bending stress concentrations in the regions in which the outer lead holes 38 are formed, thus making it possible to prevent the application of stress to the outer leads. Forming the slits before the step of forming the interconnect patterns 20 makes it possible to prevent the application of stress to the interconnect patterns 20 from the very start of their

formation.

A film carrier tape in accordance with this embodiment of the invention comprises a tape-shaped substrate (the base substrate 10) that has flexibility, punch-out regions that are set in sequence along this tape-shaped substrate, and bendable portions formed between the punch-out regions. The bending resistance between the punch-out regions is less than the bending resistance of the punch-out regions. With the film carrier tape in accordance with this embodiment of the invention, the bendable portions ensure that the bending resistance between the punch-out regions is lower. Thus, when an attempt is made to bend the film carrier tape, the bending stresses concentrate at the bendable portions, making it possible to reduce the severity of bending in the punch-out regions, with no bending stress concentrations in these punch-out regions.

The film carrier tape in accordance with this embodiment of the invention comprises a tape-shaped substrate (the base substrate 10) that has flexibility. Punch-out regions are formed in sequence along this tape-shaped substrate, and a device hole 14 is formed within each of these punch-out regions. Within each punch-out region is also formed an outer lead hole 38 adjacent to the device hole 14, and an interconnect pattern 20 which has an end portion that protrudes from the device hole 14 and another end portion that straddles the outer lead hole 38. Slits are formed by punching out between the punch-out regions. The bending resistance between the punch-out regions is made to be less than the bending resistance of regions in

which are formed the outer lead holes 38 that are straddled by the interconnect patterns 20. With the film carrier tape in accordance with this embodiment of the invention, any attempt to bend the film carrier tape applies bending stresses to the entirety thereof, but the provision of places in which slits are formed, with the weakest bending resistance, between the punch-out regions ensures that the bending stresses concentrate at those portions and the film carrier tape takes up a polygonal shape. In other words, there are no stress concentrations due to bending at the outer lead hole 38, and thus no stresses are applied to the outer leads that straddle the outer lead hole 38. This makes it possible to prevent cracking or breakage of the outer leads.

In the film carrier tape in accordance with this embodiment of the invention, the slits are formed in such a manner that the proportion occupied by the slits across the width of the tape-shaped substrate (the base substrate 10) is greater than the proportion occupied by the outer lead holes 38 across the width of the tape-shaped substrate. With the film carrier tape in accordance with this embodiment of the invention, the remaining amount of the material of the substrate is least within regions in which the slits are formed, making it possible to reduce the bending resistance thereof below that of the other regions in which the outer lead holes 38 are formed.

CLAIMS

1. A flexible interconnect substrate comprising:

a tape-shaped base substrate; and

an interconnect pattern formed on the base substrate,

wherein the base substrate includes:

a first region in which a predetermined interconnect pattern has been formed and which will form a unit when separated from the base substrate; and

a second region positioned next to the first region in the longitudinal direction of the base substrate; and

wherein the second region has a low-bending-resistance portion which is formed in a region that excludes a central portion of the second region in the widthwise direction of the base substrate, for ensuing that the second region bends more readily in the direction in which the longitudinal axis of the base substrate bends, in comparison with the first region.

2. The flexible interconnect substrate as defined in claim 1, wherein the low-bending-resistance portion is one of through-holes, cuts, and a thinner portion.

3. The flexible interconnect substrate as defined in claim 1,

wherein a high-bending-resistance portion is formed in each of the first region and the central portion of the second region in the widthwise direction of the base substrate;

wherein the high-bending-resistance portion is formed to avoid a region that excludes the central portion of the second region in the widthwise direction of the base substrate; and

wherein the region avoided by the high-bending-resistance portion forms a relatively low-bending-resistance portion.

4. The flexible interconnect substrate as defined in claim 1,

wherein a hole is formed in the first region of the base substrate; and

wherein a portion of the interconnect pattern is positioned within the hole.

5. The flexible interconnect substrate as defined in claim 4,

wherein the second region is formed to bend more readily than the first region that bends readily due to the formation of the hole.

6. The flexible interconnect substrate as defined in claim 1,

wherein a plurality of the low-bending-resistance portions are formed in a straight line within the second region, across the width of the base substrate.

7. The flexible interconnect substrate as defined in claim

6,

wherein the plurality of low-bending-resistance portions are disposed on two edge portion sides of the base substrate, symmetrically with respect to the center in the widthwise direction of the base substrate.

8. The flexible interconnect substrate as defined in claim 6,

wherein the plurality of low-bending-resistance portions are disposed on two edge portion sides of the base substrate, asymmetrically with respect to the center in the widthwise direction of the base substrate.

9. The flexible interconnect substrate as defined in claim 8,

wherein the interconnect pattern is formed to be offset towards either of two edge portions of the base substrate, with respect to the center in the widthwise direction of the base substrate.

10. A tape-shaped semiconductor device comprising:

the flexible interconnect substrate as defined in claim 1; and

a semiconductor chip connected electrically to the interconnect pattern of the base substrate.

11. A tape-shaped semiconductor device comprising:

the flexible interconnect substrate as defined in claim 8; and

a semiconductor chip which is disposed offset towards either of two edge portions of the base substrate, with respect to the center thereof in the widthwise direction of the base substrate, and which is connected electrically to the interconnect pattern of the base substrate.

12. A tape-shaped semiconductor device comprising:

the flexible interconnect substrate as defined in claim 9; and

a semiconductor chip which is disposed offset towards either of two edge portions of the base substrate, with respect to the center thereof in the widthwise direction of the base substrate, and which is connected electrically to the interconnect pattern of the base substrate.

13. A semiconductor device which has a shape obtained by punching out the base substrate of the tape-shaped semiconductor device as defined in claim 10 along an outline that surrounds the semiconductor chip.

14. A semiconductor device which has a shape obtained by punching out the base substrate of the tape-shaped semiconductor device as defined in claim 11 along an outline that surrounds the semiconductor chip.

15. A semiconductor device which has a shape obtained by punching out the base substrate of the tape-shaped semiconductor device as defined in claim 12 along an outline that surrounds the semiconductor chip.

16. A circuit board which is connected electrically to the semiconductor device defined in claim 13.

17. A circuit board which is connected electrically to the semiconductor device defined in claim 14.

18. A circuit board which is connected electrically to the semiconductor device defined in claim 15.

19. Electronic equipment having the semiconductor device as defined in claim 13.

20. Electronic equipment having the semiconductor device as defined in claim 14.

21. Electronic equipment having the semiconductor device as defined in claim 15.

22. A method of manufacturing a semiconductor device, comprising the steps of:

winding the flexible interconnect substrate as defined in any of claims 1 to 9 onto a reel in preparation; and then

pulling the flexible interconnect substrate out from the reel.

23. A method of manufacturing a semiconductor device, comprising the steps of:

winding a tape-shaped semiconductor device which comprises the flexible interconnect substrate as defined in any of claims 1 to 9 and a semiconductor chip connected electrically to the interconnect pattern of the flexible interconnect substrate, onto a reel in preparation; and then

pulling the tape-shaped semiconductor device out from the reel.

24. The method of manufacturing a semiconductor device as defined in claim 23,

wherein the flexible interconnect substrate is punched out at the first region, during the step of pulling the tape-shaped semiconductor device out from the reel.

ABSTRACT

A flexible interconnect substrate (1) comprises a tape-shaped base substrate (10) and a plurality of interconnect patterns (20) formed on the base substrate (10). The base substrate (10) has a plurality of first regions (44) set to be punched out, and second regions (45) between those first regions (44). Each of the second regions (45) has the material that forms the base substrate (10) is present in a central portion in the widthwise direction of the base substrate (10), and a low-bending-resistance portion (40) for ensuring that the second region (45) bends more readily than the adjacent first regions (44) in a direction in which the longitudinal axis of the base substrate (10) bends.

09/674924

FIG. 1

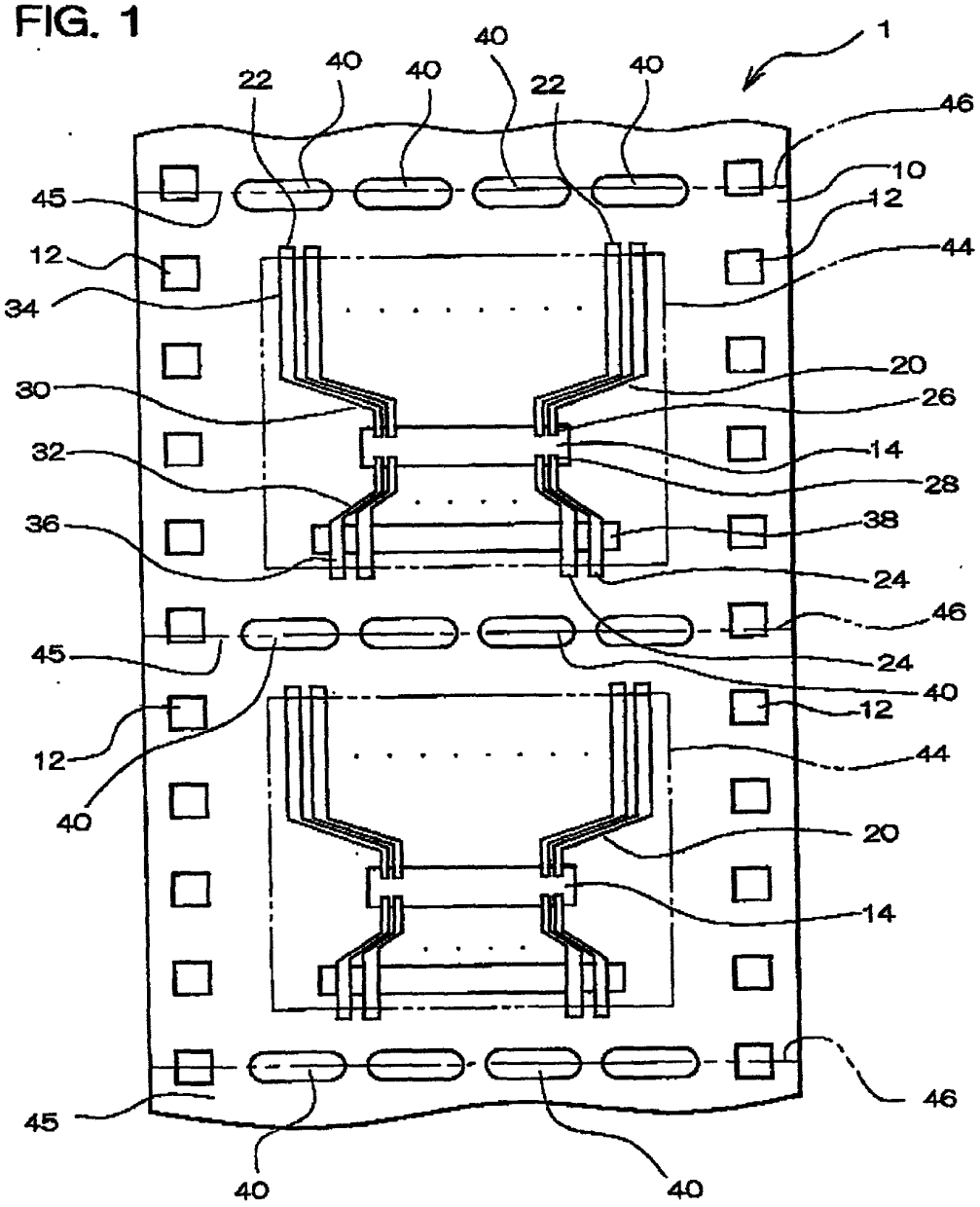


FIG. 2A

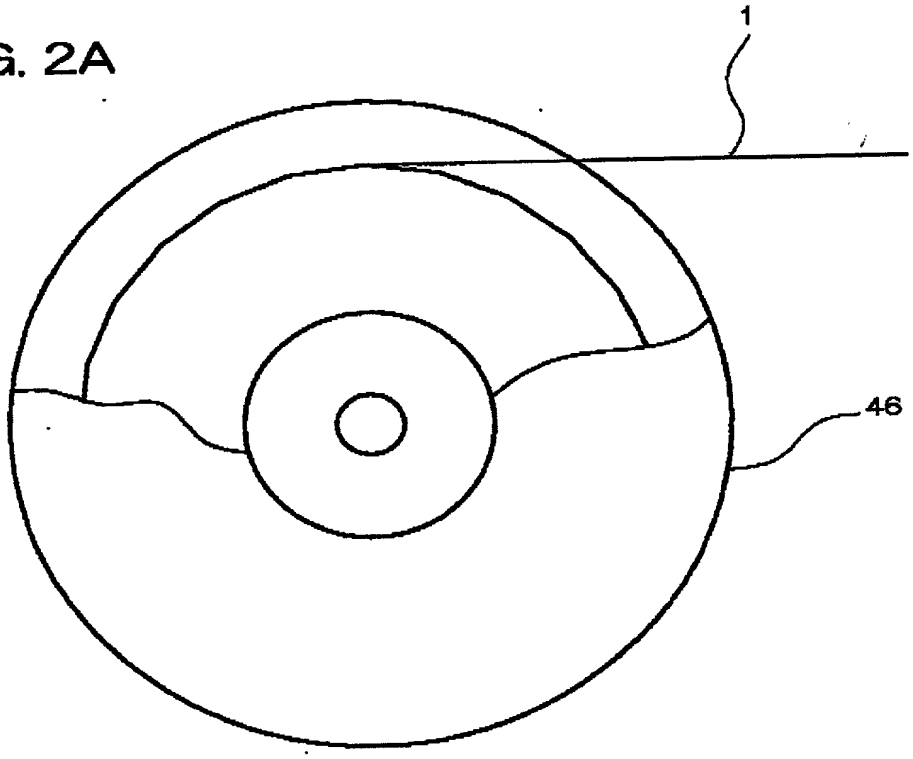


FIG.2B

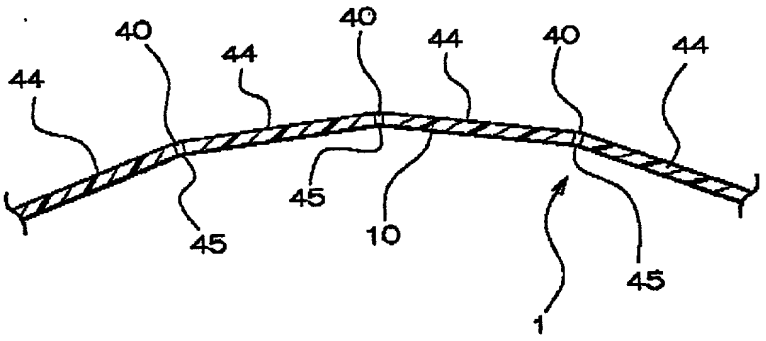


FIG. 3

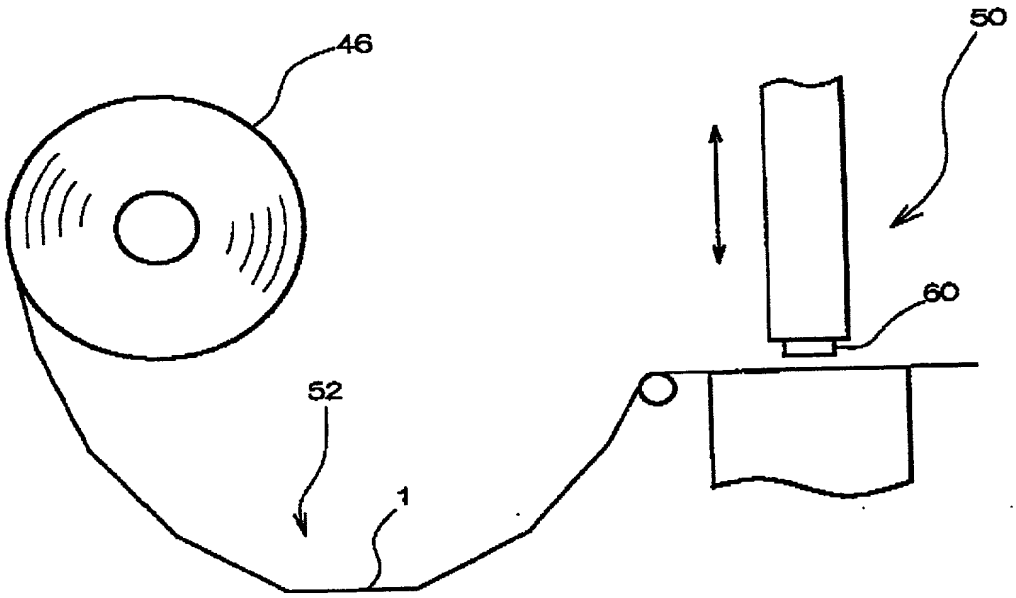


FIG. 4

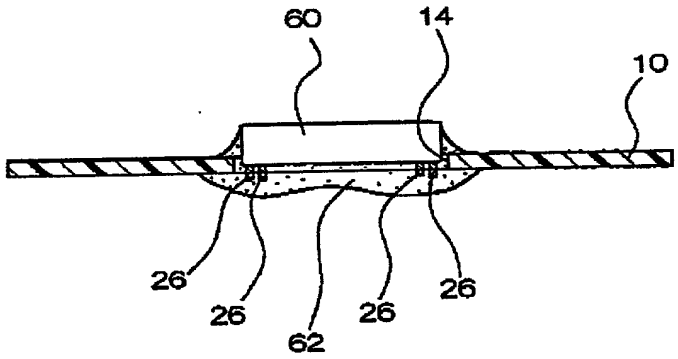


FIG. 5

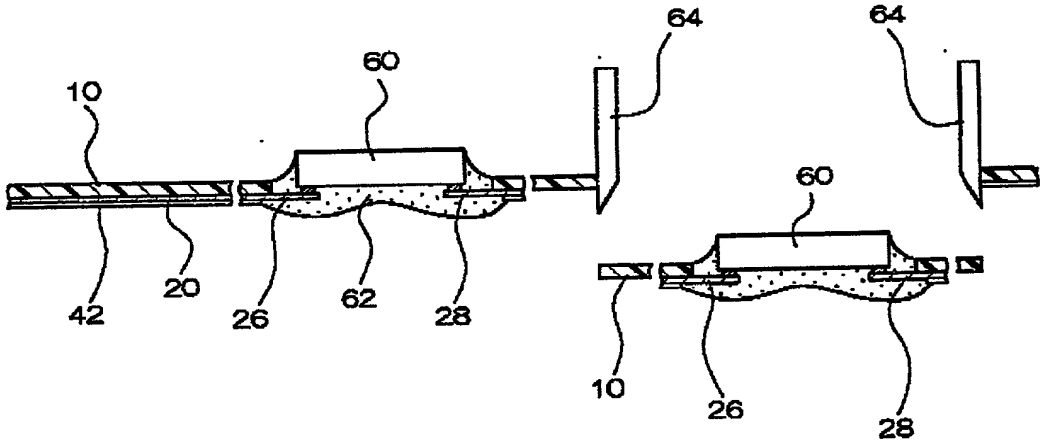


FIG. 6

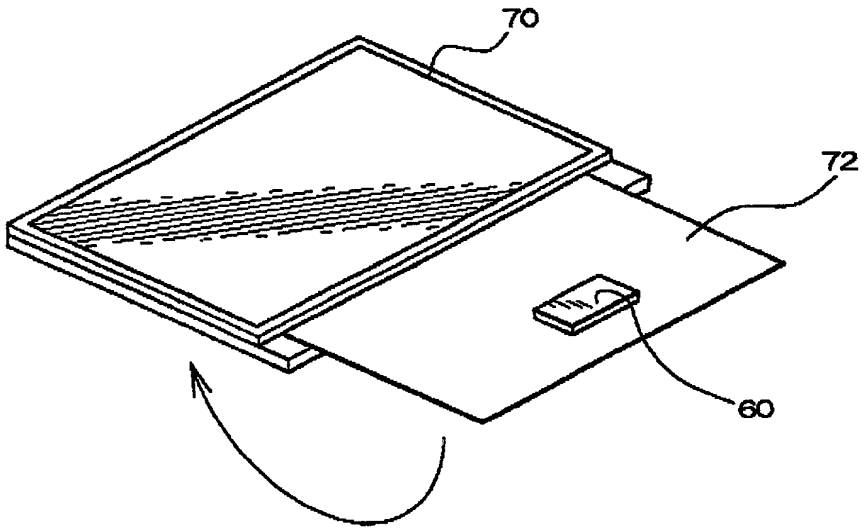


FIG. 7

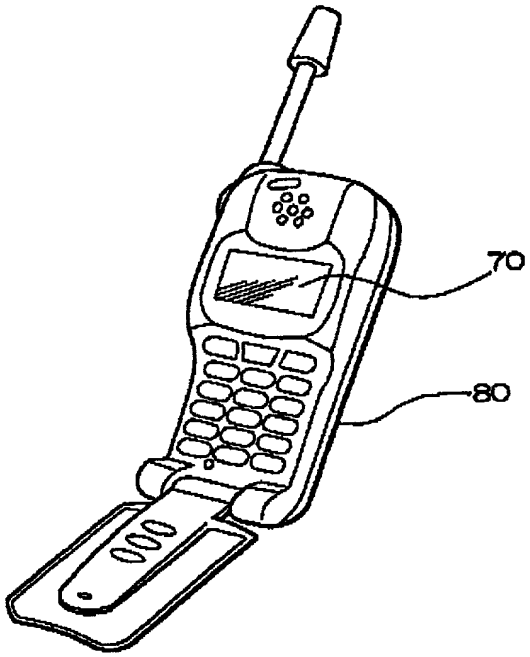


FIG. 8

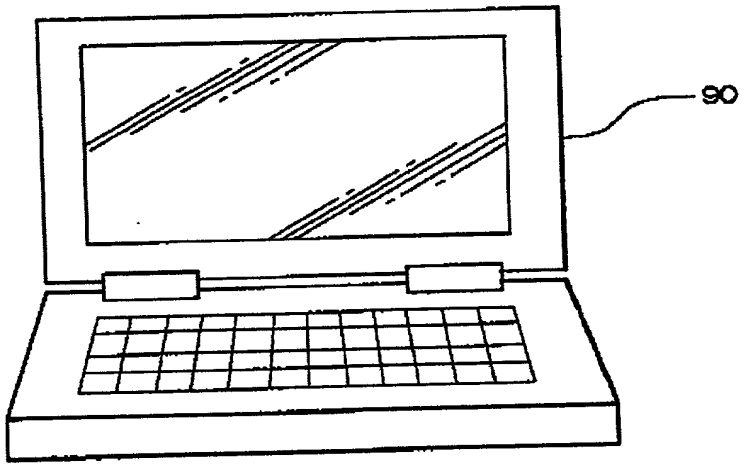


FIG. 9

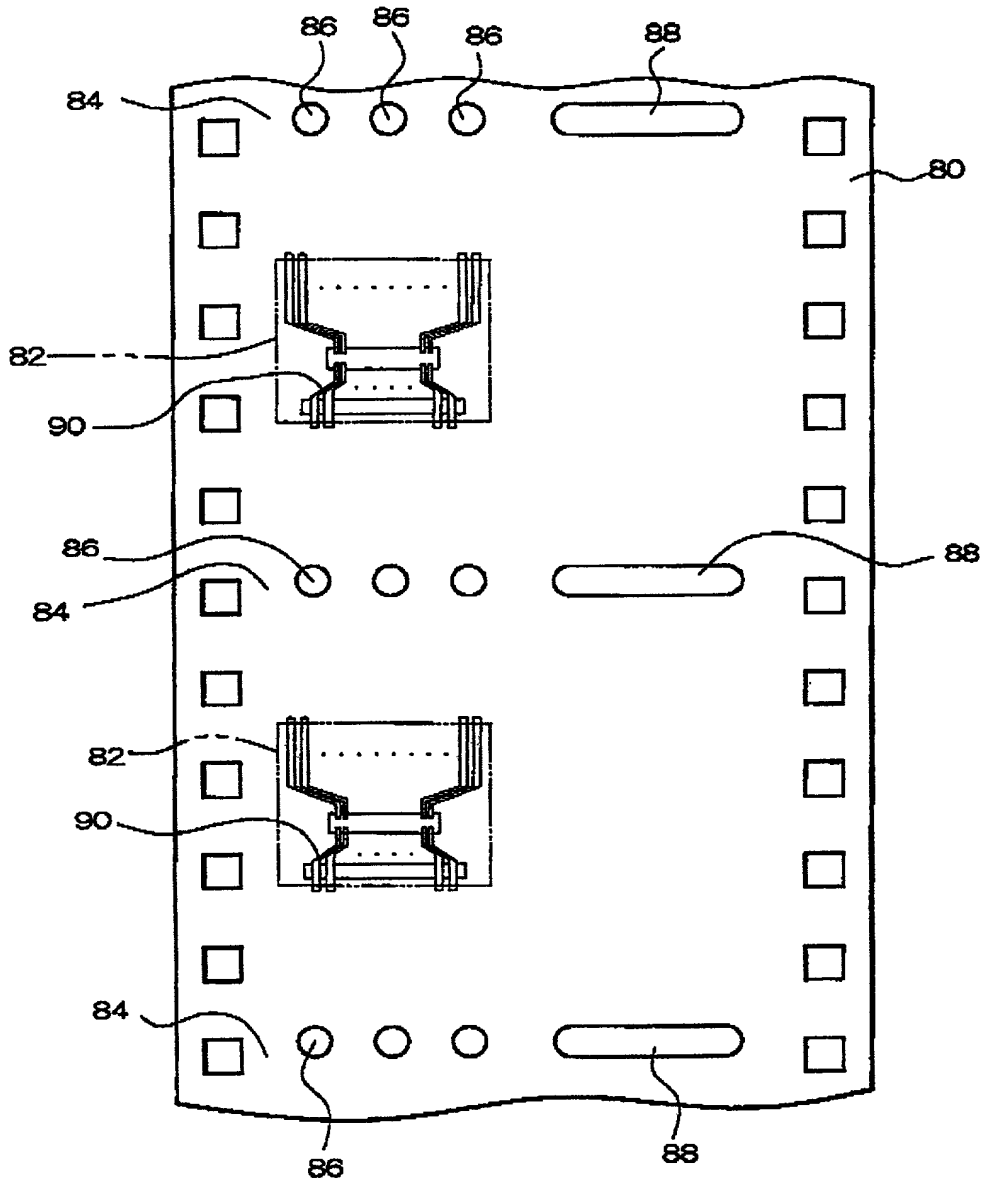


FIG. 10A

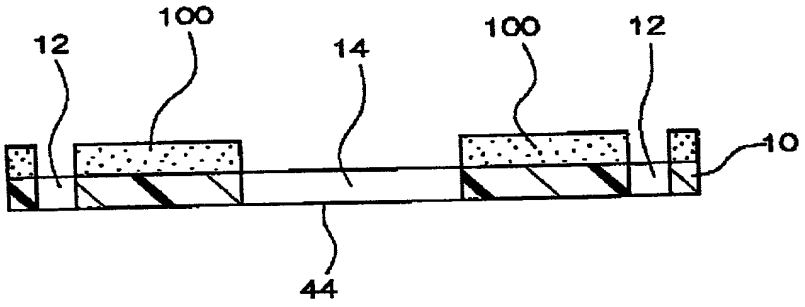
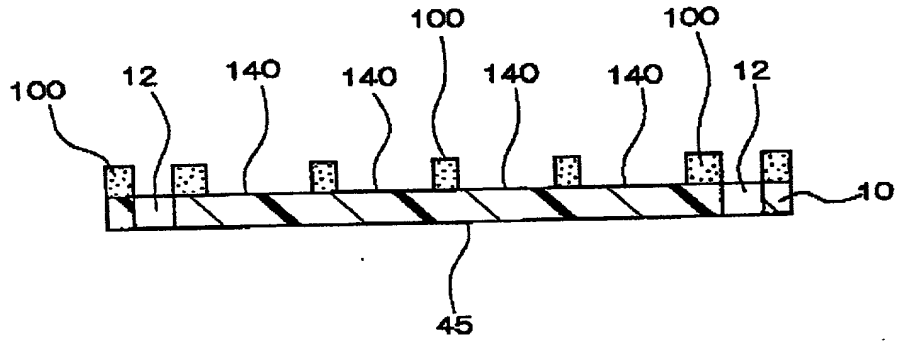


FIG. 10B



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Seiko Epson Ref. No.: F004881US00　　　**Attorney's Ref. No.:** ______

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

<u>可撓性配線基板、フィルムキャリア、テープ状半導体装置、半導体装置及びその製造方法、回路基板並びに電子機器</u>

<u>FLEXIBLE INTERCONNECT SUBSTRATE, FILM CARRIER, TAPE-SHAPED SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD AND ELECTRONIC EQUIPMENT</u>

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ______に提出され、米国出願番号または
特許協定条約 国際出願番号を ______ とし、
（該当する場合） ______ に訂正されました。

☐ was filed on ______
as United States Application Number or
PCT International Application Number
______ and was amended on
______ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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私は、米国法典第35編119条(a)－(d)項又は365条(b)項に基き下記の、米国以外の国の少なくとも1ヶ国を指定している特許協力条約365条(a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11-065226	Japan	March 11, 1999	☐
			☐

私は、第35編米国法典119条(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119 (e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

私は下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365 (c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, Section 112. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
PCT/JP00/01388	March 8, 2000	Pending

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私が入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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委任状： 私は、下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

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POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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(第三以降の共同発明者についても同様に記載し、署名をすること)	(Supply similar information and signature for third and subsequent joint inventors.)